

Client's ref.: TSMC2003-0640/

Our ref.: 0503-A30073US/final/spin(王琮郁)/Nelson

**What Is Claimed Is:**

1           1.    A semiconductor process for controlling etching  
2   profile, comprising the steps of:

3           providing a plurality of substrates, in which a film to be  
4           etched and an overlying masking pattern layer are  
5           provided overlying each substrate; and

6           etching each of the films in sequence in a plasma chamber  
7           using the masking pattern layer as an etch mask, a  
8           polymer layer being deposited over the inner wall of  
9           the plasma chamber during the etching;

10          wherein an intermediary cleaning process is performed in  
11          the plasma chamber between the etchings before the  
12          deposited polymer layer reaches such a degree as to  
13          induce lateral etching on the next film to be etched.

1           2.    The semiconductor process of claim 1, wherein the film  
2   to be etched is a silicon layer.

1           3.    The semiconductor process of claim 2, wherein the  
2   intermediary cleaning process is performed before the deposited

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3 polymer layer leads to a spectral intensity associated with the  
4 layer to be etched from OES data analysis more than 100 at a  
5 wavelength about 405 nm.

1 4. The semiconductor process of claim 1, wherein the mask  
2 layer is a silicon oxide layer.

1 5. The semiconductor process of claim 1, wherein the  
2 intermediary cleaning process is performed between each of the  
3 etchings.

1 6. The semiconductor process of claim 1, wherein the  
2 intermediary cleaning process is performed for 1~3 minutes.

1 7. The semiconductor process of claim 6, wherein the  
2 intermediary cleaning further comprises the steps of:

3 using O<sub>2</sub>, Cl<sub>2</sub>, and SF<sub>6</sub> as a first cleaning gas for about 30

4 sec; and

5 using Cl<sub>2</sub>, and HBr as a second cleaning gas for about 50

6 sec.

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1           8.    The semiconductor process of claim 1, further  
2    comprising performing a preliminary cleaning process in the  
3    plasma chamber before placing the substrates therein.

1           9.    The semiconductor process of claim 8, wherein the  
2    preliminary cleaning process is performed for 8~12 minutes.

1           10.   The semiconductor process of claim 9, wherein the  
2    preliminary cleaning process further comprises the steps of:

3           using O<sub>2</sub>, Cl<sub>2</sub>, and SF<sub>6</sub> as a first cleaning gas for about

4           70 sec;

5           using O<sub>2</sub>, Cl<sub>2</sub>, and He as a second cleaning gas for about

6           200 sec;

7           using Cl<sub>2</sub>, and HBr as a third cleaning gas for about 150

8           sec; and

9           using He as a fourth cleaning gas for about 30 sec.

1           11.   A method of forming floating gates for flash memory  
2    devices, comprising the steps of:

3           providing a substrate;

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4            successively forming a floating gate dielectric layer and  
5            a polysilicon layer overlying each of the substrate;  
6            forming a capping layer with a bird's beak overlying the  
7            polysilicon layer; and  
8            etching each of the polysilicon layers in sequence in a  
9            plasma chamber using the overlying capping layer as  
10           an etch mask to form a floating gate on each of the  
11           floating gate dielectric layers, a polymer layer  
12           being deposited over the inner wall of the plasma  
13           chamber during the etching;  
14           wherein an intermediary cleaning process is performed in  
15           the plasma chamber between the etchings before the  
16           deposited polymer layer reaches such a degree as to  
17           induce lateral etching on the next polysilicon layer.

1           12. The method of claim 11, wherein the intermediary  
2           cleaning process is performed between each of the etchings.

1           13. The method of claim 11, the intermediary cleaning  
2           process is performed for 1~3 minutes.

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1           14. The method of claim 13, wherein the intermediary  
2 cleaning process further comprises the steps of:  
3           using O<sub>2</sub>, Cl<sub>2</sub>, and SF<sub>6</sub> as a first cleaning gas to perform  
4           the for about 30 sec; and  
5           using Cl<sub>2</sub>, and HBr as a second cleaning gas to perform the  
6           for about 50 sec.

1           15. The method of claim 11, further comprising performing  
2 a preliminary cleaning process in the plasma chamber before  
3 placing the substrates therein.

1           16. The method of claim 15, wherein the preliminary  
2 cleaning process is performed for 8~12 minutes.

1           17. The method of claim 16, wherein the preliminary  
2 cleaning process further comprises the steps of:  
3           using O<sub>2</sub>, Cl<sub>2</sub>, and SF<sub>6</sub> as a first cleaning gas for about  
4           70 sec;  
5           using O<sub>2</sub>, Cl<sub>2</sub>, and He as a second cleaning gas for about  
6           200 sec;

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7           using Cl<sub>2</sub>, and HBr as a third cleaning gas   for about 150  
8                   sec; and  
9           using He as a fourth cleaning gas   for about 30 sec.

1           18. The method of claim 11, wherein the intermediary  
2   cleaning process is performed before the deposited polymer layer  
3   leads to a spectral intensity associated with the polysilicon  
4   layer from OES data analysis more than 100 at a wavelength about  
5   405 nm.

1           19. The method of claim 11, wherein the floating gate  
2   dielectric layer is a silicon oxide layer.

1           20. The method of claim 11, wherein the capping layer is  
2   silicon oxide layer.

1           21. A method of forming floating gates for flash memory  
2   devices, comprising the steps of:

3           providing a plurality of substrates;  
4           successively forming a floating gate oxide layer and a  
5           polysilicon layer overlying each of the substrates;

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6           forming a oxide layer with a bird's beak overlying the  
7           polysilicon layer; and  
8           etching each of the polysilicon layers in sequence in a  
9           cleaned plasma chamber using the overlying oxide  
10          layer as an etch mask to form a floating gate on each  
11          of the floating gate oxide layers, a polymer layer  
12          being deposited over the inner wall of the plasma  
13          chamber during the etching;  
14          wherein a cleaning process is performed in the plasma  
15          chamber between each of the etchings to remove the  
16          deposited polymer layer.

1          22. The method of claim 21, wherein the cleaning process  
2          is performed for 1~3 minutes.

1          23. The method of claim 22, wherein the cleaning process  
2          further comprises the steps of:

3           using  $O_2$ ,  $Cl_2$ , and  $SF_6$  as a first cleaning gas for about 30  
4           sec; and

5           using  $Cl_2$ , and HBr as a second cleaning gas for about 50  
6          sec.